intel

Intel486™ FAMILY OF MICROPROCESSORS
LOW POWER VERSION
DATA SHEET

Low Power Intel486™ SX CPU/Intel487™ SX MCP
Low Power Intel486 DX CPU

- **Lower Power Dissipation**
  - **Dynamic Frequency Scalability**
  - **I_{CC}(max) Reduced to 150 mA at 2 MHz**
  - **Improved V_{CC} Rating (± 10%)**
- **Binary Compatible with Large Software Base**
  - **MS-DOS*, OS/2**, Windows***
  - **UNIX*** System V/386**
  - **iRMX®, iRMK Kernels**
- **High Integration Enables On-Chip**
  - **8 KByte Code and Data Cache**
  - **Floating Point Unit on the Intel486 DX CPU and Intel487™ SX Math CoProcessor**
  - **Paged, Virtual Memory Management**
- **Easy to Use**
  - **Built-In Self Test**
  - **Hardware Debugging Support**
  - **Intel Software Support**
  - **Extensive Third Party Software Support**
- **168-Lead Pin Grid Array Package for Intel486 DX Microprocessor**
- **168-Lead Pin Grid Array for Intel486™ SX Microprocessor**
- **196-Lead Plastic Quad Flat Package for Intel486™ SX Microprocessor**
- **169-Pin Grid Array Package for Intel487™ SX Math CoProcessor**
- **High Performance Design**
  - **Intel486™ One Clock Instruction Core**
  - **16/20/25 MHz Operation for Intel486™ SX**
  - **25 MHz Operation for Intel486™ DX**
  - **64 MByte/Sec Burst Bus**
  - **CHMOS IV Process Technology**
  - **Dynamic Bus Sizing for 8-, 16- and 32-Bit Buses**
- **Complete 32-Bit Architecture**
  - **Address and Data Buses**
  - **Registers**
  - **8-, 16- and 32-Bit Data Types**
- **Multiprocessor Support**
  - **Multiprocessor Instructions**
  - **Cache Consistency Protocols**
  - **Support for Second Level Cache**

The data sheet describes both the Low Power Intel486 SX and the Low Power Intel486 DX microprocessors. The Intel487 SX Math CoProcessor will support the low power Intel486 SX microprocessor as an optional upgrade available through the retail channel.

The Low Power Intel486 family microprocessors meet today's need for high performance portables. Their combination of special features like dynamic frequency scaling, lower minimum frequency, improved V_{CC} operation and high integration contribute significantly to lower power dissipation and meet the needs of portable computing.

The Low Power capability is achieved by operating the Intel486 microprocessor in the 2X mode. The frequency can be varied dynamically between maximum to minimum as needed. The frequency change does not affect contents of the registers and data integrity is maintained. Power dissipation is reduced significantly at 2 MHz where I_{CC} is only 150 mA compared to 600 mA at 20 MHz. Low power versions are offered for both the Intel486 SX and the Intel486 DX microprocessors.

The Low Power Intel486 microprocessors are 100-percent compatible with all versions of the Intel386™ microprocessor family, assuring compatibility with the more than $40 billion software base of MS-DOS, Windows, OS/2 and UNIX/System operating system applications. The Low Power Intel486 microprocessor integrates the same RISC-technology, one clock per instruction integer core, on-chip cache, and memory management unit as the standard Intel486 microprocessor.

The Intel487 SX Math CoProcessor provides optional math upgrade capability for the Intel486 SX microprocessor and supports low power operation; providing end-users increased floating point performance for more than 2100 software packages that were designed to use Intel Math CoProcessors. Note that the Intel OverDrive™ Processor does not work in systems based on the Low Power Intel486 CPU.

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**OS/2 is a trademark of International Business Machines.
***UNIX is a trademark of UNIX Systems Laboratories.

December 1992
Order Number: 241199-002

Intel486™ Family of Microprocessors
Low Power Version
Data Sheet

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CONTENTS

This document should be used in conjunction with the Intel486™ DX Microprocessor data sheet (order number 240440-004, June 1991) and the Intel486™ SX Microprocessor data sheet (order number 240950-002, October 1991).

1.0 INTRODUCTION

The Low Power Intel486 microprocessor brings Intel486 technology and performance to the portable computer market. The low power capability is achieved by a frequency scalability feature during normal operation. The operating frequency can be brought down dynamically resulting in lower power supply current (I_{CC}). This results in minimal power dissipation which ensures a longer battery life.

The Low Power Intel486 microprocessor integrates the same RISC-technology, one clock per instruction integer core, on-chip cache, and memory management unit as the standard Intel486 microprocessor.

The Low Power Intel486 microprocessor has the following special features:

- **Frequency Scalability**—This is achieved by operating the Intel486 microprocessor in the 2X clock mode. The frequency can be varied dynamically from maximum back to minimum or vice versa. The frequency change does not affect the register content of the CPU, thus data integrity is maintained.
- **Lower Minimum Frequency**—The Low Power Intel486 microprocessor can be operated at a minimum frequency of 2 MHz, at which I_{CC}(max) is only 150 mA, compared to an I_{CC}(max) of 600 mA at 20 MHz operation. The power dissipation is thus drastically reduced ensuring a longer battery life.
- **Improved V_{CC} Operation**—The Low Power Intel486 microprocessor has an improved V_{CC} rating of ±10%. Again this feature makes it extremely attractive to portable battery powered applications.

The above three features ensure power savings for portable computer systems resulting in prolonged battery life.

Besides the above special features, the Low Power Intel486 microprocessor has an identical feature set to the standard Intel486 CPU. This includes:

- **Binary Compatibility**—The Low Power Intel486 CPU is binary compatible with the 8086, 8088, 80186, 80286, i386™ SX, i386™ DX, Intel486™ SX and Intel486™ DX CPUs.
- **Full 32-Bit Integer Processor**—The Low Power Intel486 CPU performs a complete set of arithmetic and logical operations on 8-, 16-, and 32-bit data types using a full-width ALU and eight general-purpose registers.
- **Separate 32-Bit Address and Data Paths**—Four gigabytes of physical memory can be addressed directly.
- **Single-Cycle Execution**—Many instructions execute in a single clock cycle.
- **On-Chip Floating Point Unit**—This is available on the Intel486 DX CPU. The 32-, 64-, and 80-bit formats specified in IEEE standard 754 are supported. The unit is binary compatible with the 8087, 80287, i387™, i387™ SX, and Intel487™ math coprocessors and the Intel486™ CPU.
- **On-Chip Memory Management Unit**—Address-management and memory-space protection mechanisms maintain the integrity of memory. This is necessary in multitasking and virtual-memory environments, like those implemented by the UNIX and OS/2 operating systems. Both memory segmentation and paging are supported.
- **On-Chip Cache with Cache Consistency Support**—The internal write-through cache can hold 8 KBytes of data or instructions. Cache hits are as fast as read accesses to a processor register. Bus activity is tracked to detect alterations in the memory which internal cache represents. The internal cache can be invalidated or flushed, so that an external cache controller can maintain cache consistency in multi-processor environments.
- **External Cache Control**—Write-back and flush controls over an external cache are provided so that the processor can maintain cache consistency in multi-processor environments.
- **Instruction Pipelining**—The fetching, decoding, execution and address translation of instructions are overlaped within the Low Power Intel486 microprocessor. This results in a continuous execution rate of one clock cycle per instruction, for most instructions.
- **Burst Cycles**—Burst transfers allow a new doubleword to be read from memory each clock cycle. With this capability the internal cache and instruction prefetch buffer can be filled very rapidly.
- **Write Buffers**—The processor contains write buffers to enhance the performance of consecutive writes to memory. The Low Power Intel486 CPU can continue operations internally after a write, without waiting for the write to be executed on the external bus.
- **Bus Backoff**—If another bus master needs control of the bus during a Low Power Intel486 microprocessor initiated bus cycle, the Low Power

Intel486 microprocessor will float its bus signals, then restart its cycle when the bus becomes available again.

- **Instruction Restart**—Programs can continue execution following an exception generated by an unsuccessful attempt to access memory. This feature is important for supporting demand-paged virtual memory applications.
- **Dynamic Bus Sizing**—External controllers can dynamically alter the effective width of the data bus. Bus widths of 8, 16 or 32 bits can be used.

1.1 Pinout

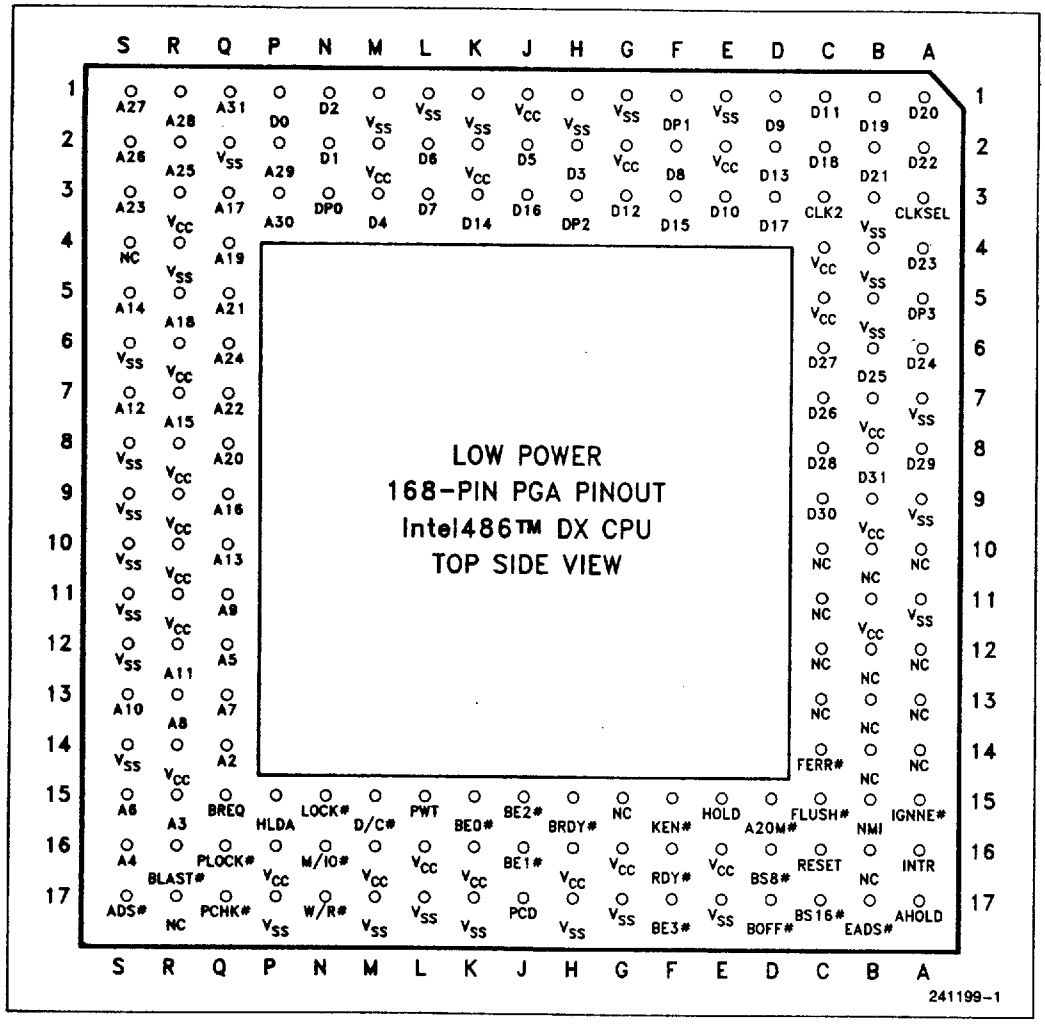


Figure 1-1. Low Power Intel486™ DX CPU Pinout (Top Side View)

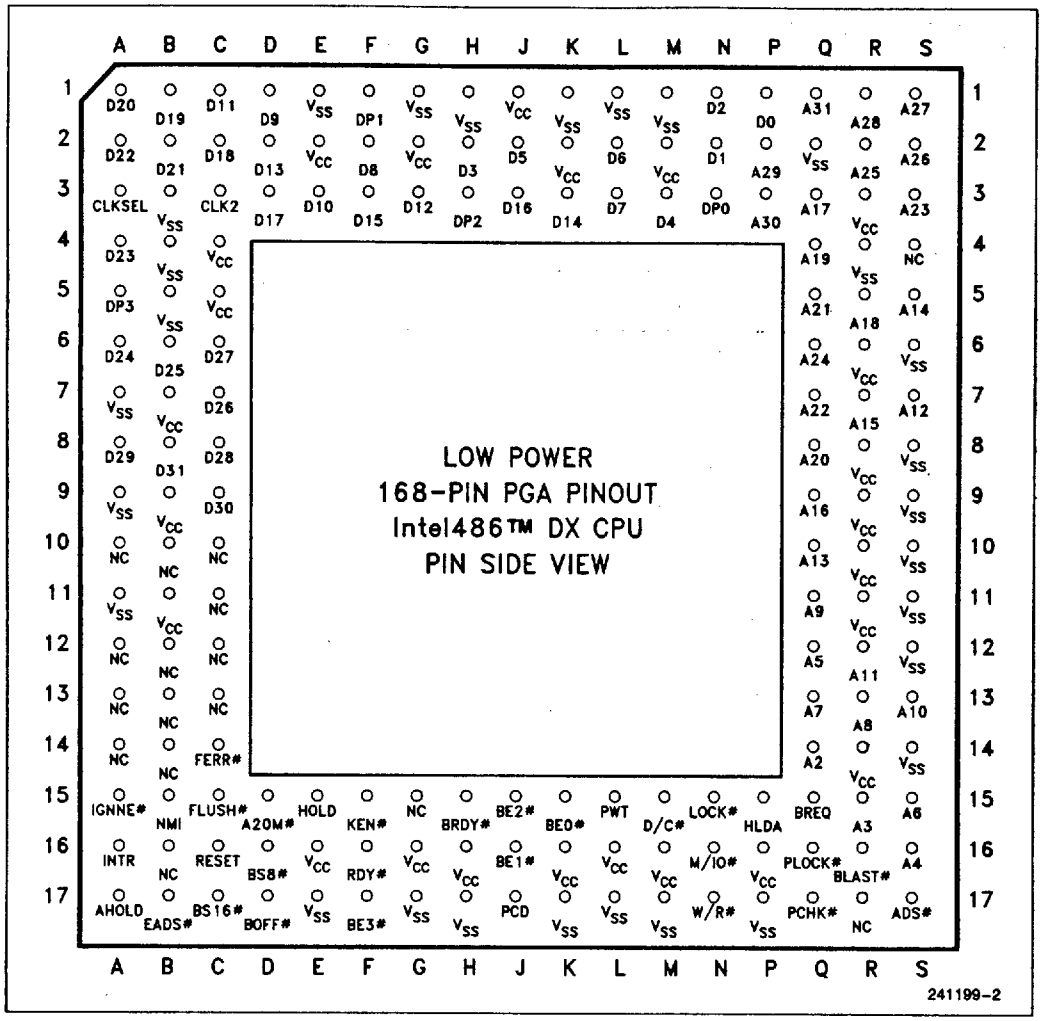


Figure 1-2. Low Power Intel486™ DX CPU Pinout (Pin Side View)

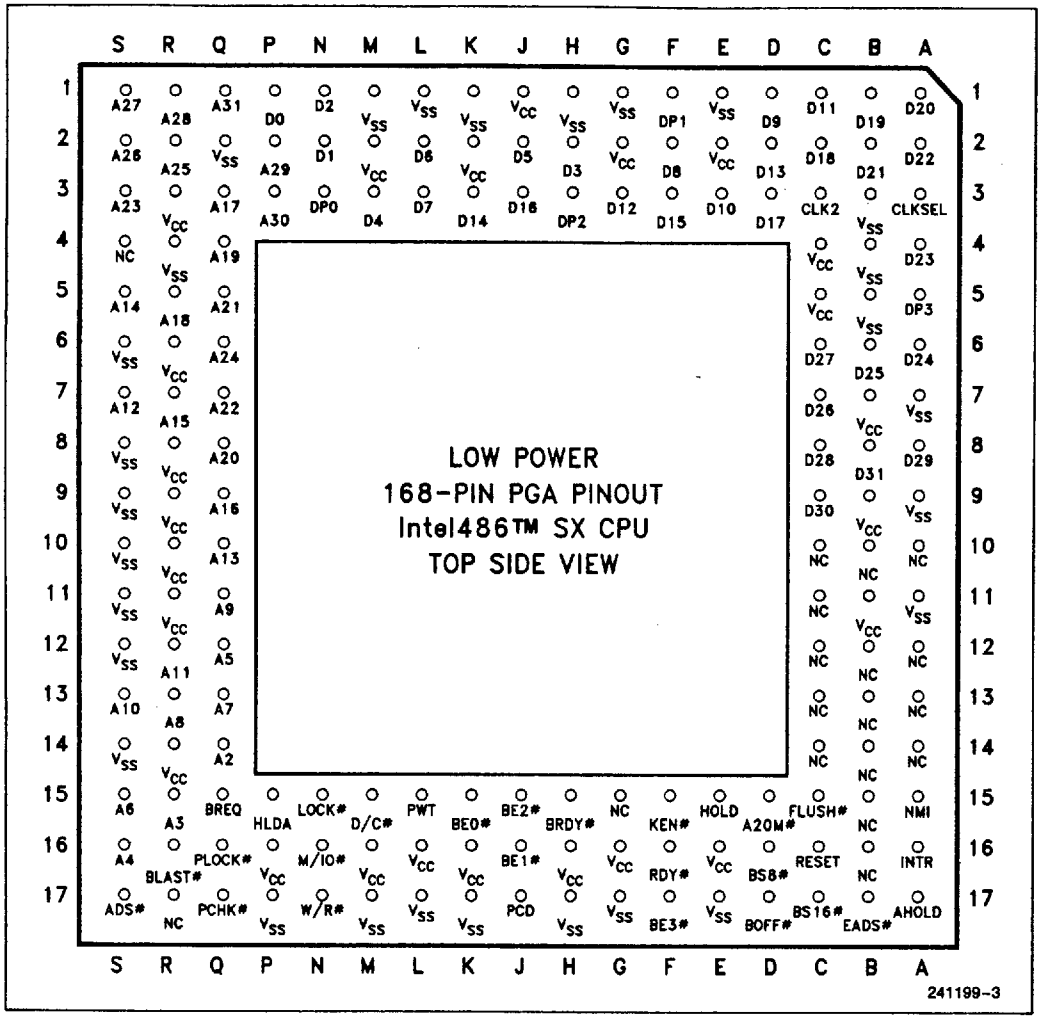


Figure 1-3. Low Power Intel486™ SX CPU Pinout (Top Side View)

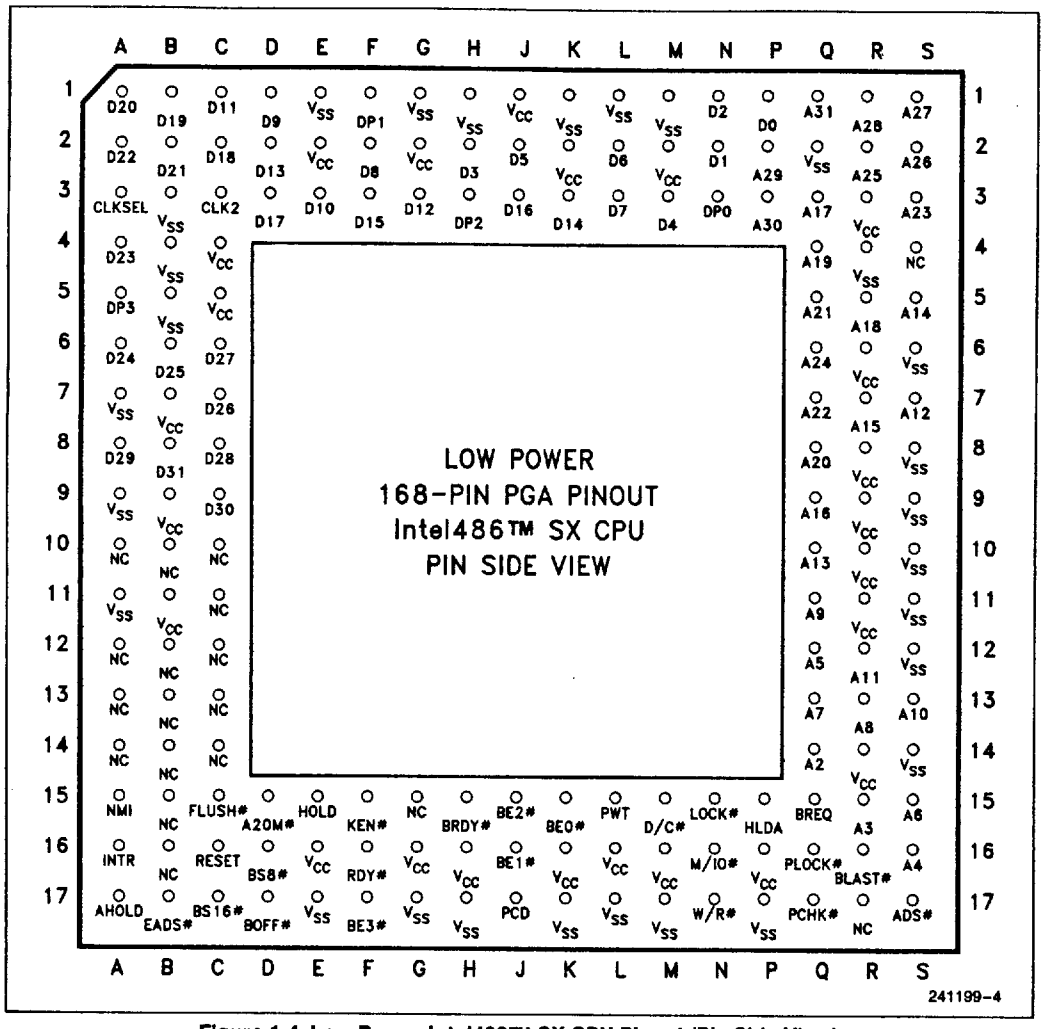


Figure 1-4. Low Power Intel486™ SX CPU Pinout (Pin Side View)

Figure 1-5. Low Power Intel486™ SX CPU 196-Lead PQFP Pinout

1.2 Pin Cross Reference (Intel486™ DX CPU)

Address		Data		Control		N/C	V_{CC}	V_{SS}
A_2	Q14	D_0	P1	A20M#	D15	A10	B7	A7
A_3	R15	D_1	N2	ADS#	S17	A12	B9	A9
A_4	S16	D_2	N1	AHOLD	A17	A13	B11	A11
A_5	Q12	D_3	H2	BE0#	K15	A14	C4	B3
A_6	S15	D_4	M3	BE1#	J16	B10	C5	B4
A_7	Q13	D_5	J2	BE2#	J15	B12	E2	B5
A_8	R13	D_6	L2	BE3#	F17	B13	E16	E1
A_9	Q11	D_7	L3	BLAST#	R16	B14	G2	E17
A_{10}	S13	D_8	F2	BOFF#	D17	B16	G16	G1
A_{11}	R12	D_9	D1	BRDY#	H15	C10	H16	G17
A_{12}	S7	D_{10}	E3	BREQ	Q15	C11	J1	H1
A_{13}	Q10	D_{11}	C1	BS8#	D16	C12	K2	H17
A_{14}	S5	D_{12}	G3	BS16#	C17	C13	K16	K1
A_{15}	R7	D_{13}	D2	CLK2	C3	G15	L16	K17
A_{16}	Q9	D_{14}	K3	CLKSEL	A3	R17	M2	L1
A_{17}	Q3	D_{15}	F3	D/C#	M15	S4	M16	L17
A_{18}	R5	D_{16}	J3	DP0	N3		P16	M1
A_{19}	Q4	D_{17}	D3	DP1	F1		R3	M17
A_{20}	Q8	D_{18}	C2	DP2	H3		R6	P17
A_{21}	Q5	D_{19}	B1	DP3	A5		R8	Q2
A_{22}	Q7	D_{20}	A1	EADS#	B17		R9	R4
A_{23}	S3	D_{21}	B2	FERR#	C14		R10	S6
A_{24}	Q6	D_{22}	A2	FLUSH#	C15		R11	S8
A_{25}	R2	D_{23}	A4	HLDA	P15		R14	S9
A_{26}	S2	D_{24}	A6	HOLD	E15			S10
A_{27}	S1	D_{25}	B6	IGNNE#	A15			S11
A_{28}	R1	D_{26}	C7	INTR	A16			S12
A_{29}	P2	D_{27}	C6	KEN#	F15			S14
A_{30}	P3	D_{28}	C8	LOCK#	N15			
A_{31}	Q1	D_{29}	A8	M/IO#	N16			
		D_{30}	C9	NMI	B15			
		D_{31}	B8	PCD	J17			
				PCHK#	Q17			
				PWT	L15			
				PLOCK#	Q16			
				RDY#	F16			
				RESET	C16			
				W/R#	N17			

1.3 Pin Cross Reference (Intel486™ SX CPU)

Address		Data		Control		N/C	V_{CC}	V_{SS}
A_2	Q14	D_0	P1	A20M#	D15	A10	B7	A7
A_3	R15	D_1	N2	ADS#	S17	A12	B9	A9
A_4	S16	D_2	N1	AHOLD	A17	A13	B11	A11
A_5	Q12	D_3	H2	BE0#	K15	A14	C4	B3
A_6	S15	D_4	M3	BE1#	J16	B10	C5	B4
A_7	Q13	D_5	J2	BE2#	J15	B12	E2	B5
A_8	R13	D_6	L2	BE3#	F17	B13	E16	E1
A_9	Q11	D_7	L3	BLAST#	R16	B14	G2	E17
A_{10}	S13	D_8	F2	BOFF#	D17	B15	G16	G1
A_{11}	R12	D_9	D1	BRDY#	H15	B16	H16	G17
A_{12}	S7	D_{10}	E3	BREQ	Q15	C10	J1	H1
A_{13}	Q10	D_{11}	C1	BS8#	D16	C11	K2	H17
A_{14}	S5	D_{12}	G3	BS16#	C17	C12	K16	K1
A_{15}	R7	D_{13}	D2	CLK2	C3	C13	L16	K17
A_{16}	Q9	D_{14}	K3	CLKSEL	A3	C14	M2	L1
A_{17}	Q3	D_{15}	F3	D/C#	M15	G15	M16	L17
A_{18}	R5	D_{16}	J3	DP0	N3	R17	P16	M1
A_{19}	Q4	D_{17}	D3	DP1	F1	S4	R3	M17
A_{20}	Q8	D_{18}	C2	DP2	H3		R6	P17
A_{21}	Q5	D_{19}	B1	DP3	A5		R8	Q2
A_{22}	Q7	D_{20}	A1	EADS#	B17		R9	R4
A_{23}	S3	D_{21}	B2	FLUSH#	C15		R10	S6
A_{24}	Q6	D_{22}	A2	HLDA	P15		R11	S8
A_{25}	R2	D_{23}	A4	HOLD	E15		R14	S9
A_{26}	S2	D_{24}	A6	INTR	A16			S10
A_{27}	S1	D_{25}	B6	KEN#	F15			S11
A_{28}	R1	D_{26}	C7	LOCK#	N15			S12
A_{29}	P2	D_{27}	C6	M/IO#	N16			S14
A_{30}	P3	D_{28}	C8	NMI	B15			
A_{31}	Q1	D_{29}	A8	PCD	J17			
		D_{30}	C9	PCHK#	Q17			
		D_{31}	B8	PWT	L15			
				PLOCK#	Q16			
				RDY#	F16			
				RESET	C16			
				W/R#	N17			

1.4 Pin Cross Reference by Signal Type (Intel486™ SX PQFP CPU)

Address		Data		Control		N/C	V_{CC}	V_{SS}
A_2	146	D_0	17	A20M#	104	15	6	1
A_3	150	D_1	18	ADS#	145	34	19	11
A_4	152	D_2	20	AHOLD	129	52	24	21
A_5	154	D_3	23	BE0#	117	56	28	22
A_6	158	D_4	25	BE1#	116	60	36	33
A_7	159	D_5	26	BE2#	115	64	49	40
A_8	161	D_6	27	BE3#	113	68	54	50
A_9	163	D_7	29	BLAST#	144	72	62	58
A_{10}	165	D_8	31	BOFF#	137	73	70	66
A_{11}	172	D_9	32	BRDY#	138	75	84	86
A_{12}	174	D_{10}	35	BREQ	118	76	93	95
A_{13}	176	D_{11}	37	BS8#	135	77	98	96
A_{14}	178	D_{12}	38	BS16#	136	78	107	99
A_{15}	180	D_{13}	39	CLK2	123	79	112	109
A_{16}	181	D_{14}	41	CLKSEL	127	81	119	114
A_{17}	183	D_{15}	42	D/C#	110	82	125	121
A_{18}	189	D_{16}	44	DP0	16	83	131	126
A_{19}	191	D_{17}	45	DP1	30	85	147	141
A_{20}	193	D_{18}	46	DP2	43	87	164	148
A_{21}	2	D_{19}	47	DP3	57	88	170	167
A_{22}	3	D_{20}	48	EADS#	105	89	175	168
A_{23}	4	D_{21}	51	FLUSH#	102	90	179	177
A_{24}	5	D_{22}	53	HLDA	122	91	184	182
A_{25}	7	D_{23}	55	HOLD	130	92	196	194
A_{26}	8	D_{24}	59	INTR	101	94		
A_{27}	9	D_{25}	61	KEN#	132	97		
A_{28}	10	D_{26}	63	LOCK#	142	124		
A_{29}	12	D_{27}	65	M/IO#	111	134		
A_{30}	13	D_{28}	67	NMI	100	140		
A_{31}	14	D_{29}	69	PCD	106	149		
		D_{30}	71	PCHK#	139	151		
		D_{31}	74	PWT	108	153		
				PLOCK#	143	155		
				RDY#	133	157		
				RESET	103	160		
				TCK	128	162		
				TDI	185	166		
				TDO	80	166		
				TMS	187	169		
				UP#	156	171		
				W/R#	120	173		
						186		
						188		
						190		
						192		
						195		

1.5 Pin Description

The following table provides brief pin descriptions.

Symbol	Type	Name and Function
CLK2	I	**CLK2** provides the fundamental timing for the Low Power Intel486 microprocessor. This is twice the internal frequency of the CPU.
CLKSEL	I	**Clock Select** pin selects the 2X mode required for the Low Power Intel486 CPU. A well defined pulse on this pin establishes the phase relationship of the 2X clock. With the exception of a pulse during cold reset, this pin should be driven low all the time and must be free of spikes or glitches.
ADDRESS BUS		
A31–A4 A3–A2	I/O O	A31–A2 are the **address lines** of the microprocessor. A31–A2, together with the byte enables BE0#–BE3#, define the physical area of memory or input/output space accessed. Address lines A31–A4 are used to drive addresses into the microprocessor to perform cache line invalidations. Input signals must meet setup and hold times t_{22} and t_{23}. A31–A2 are not driven during bus or address hold.
BE0–3#	O	The **byte enable** signals indicate active bytes during read and write cycles. During the first cycle of a cache fill, the external system should assume that all byte enables are active. BE3# applies to D24–D31, BE2# applies to D16–D23, BE1# applies to D8–D15 and BE0# applies to D0–D7. BE0#–BE3# are active LOW and are not driven during bus hold.
DATA BUS		
D31–D0	I/O	These are the **data lines** for the Low Power Intel486 micrprocessor. Lines D0–D7 define the least significant byte of the data bus while lines D24–D31 define the most significant byte of the data bus. These signals must meet setup and hold times t_{22} and t_{23} for proper operation on reads. These pins are driven during the second and subsequent clocks of write cycles.
DATA PARITY		
DP0–DP3	I/O	There is one **data parity** pin for each byte of the data bus. Data parity is generated on all write data cycles with the same timing as the data driven by the Low Power Intel486 microprocessor. Even parity information must be driven back into the microprocessor on the data parity pins with the same timing as read information to insure that the correct parity check status is indicated by the Low Power Intel486 microprocessor. The signals read on these pins do not affect program execution. Input signals must meet setup and hold times t_{22} and t_{23}. DP0–DP3 should be connected to V_{CC} through a pullup resistor in systems which do not use parity. DP0–DP3 are active HIGH and are driven during the second and subsequent clocks of write cycles.
PCHK#	O	**Parity Status** is driven on the PCHK# pin the clock after ready for read operations. The parity status is for data sampled at the end of the previous clock. A parity error is indicated by PCHK# being LOW. Parity status is only checked for enabled bytes as indicated by the byte enable and bus size signals. PCHK# is valid only in the clock immediately after read data is returned to the microprocessor. At all other times PCHK# is inactive (HIGH). PCHK# is never floated.

1.5 Pin Description (Continued)

Symbol	Type	Name and Function
BUS CYCLE DEFINITION		
M/IO# D/C# W/R#	O O O	The **memory/input-output**, **data/control** and **write/read** lines are the primary bus definitions signals. These signals are driven valid as the ADS# signal is asserted.
		M/IO# D/C# W/R# Bus Cycle Initiated 0 0 0 Interrupt Acknowledge 0 0 1 Halt/Special Cycle 0 1 0 I/O Read 0 1 1 I/O Write 1 0 0 Code Read 1 0 1 Reserved 1 1 0 Memory Read 1 1 1 Memory Write
		The bus definition signals are not driven during bus hold and follow the timing of the address bus.
LOCK#	O	The **bus lock** pin indicates that the current bus cycle is locked. The Low Power Intel486 microprocessor will not allow a bus hold when LOCK# is asserted (but address holds are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the last clock of the last locked bus cycle. The last locked cycle ends when ready is returned. LOCK# is active LOW and is not driven during bus hold. Locked read cycles will not be transformed into cache fill cycles if KEN# is returned active.
PLOCK#	O	The **pseudo-lock#** pin indicates that the current bus transaction requires more than one bus cycle to complete. Examples of such operations are segment table reads (64 bits), cache line fills (128 bits). The Low Power Intel486 microprocessor will drive PLOCK# active until the addresses for the last bus cycle of the transaction have been driven regardless of whether RDY# or BRDY# have been returned. Normally PLOCK# and BLAST# are inverse of each other. PLOCK# is a function of the BS8#, BS16# and KEN# inputs. PLOCK# should be sampled only if the clock ready is returned. PLOCK# is active LOW and is not driven during bus hold.
BUS CONTROL		
ADS#	O	The **address status** output indicates that a valid bus cycle definition and address are available on the cycle definition lines and address bus. ADS# is driven active in the same clock as the addresses are driven. ADS# is active LOW and is not driven during bus hold.
RDY#	I	The **non-burst Ready** input indicates that the current bus cycle is complete. RDY# indicates that the external system has presented valid data in response to a read or that the external system has accepted data in response to a write. RDY# is ignored when the bus is idle and at the end of the first clock in a bus cycle. RDY# is active during address hold. Data can be returned to the processor while AHOLD is active. RDY# is active LOW and is provided with a small pullup resistor. RDY# must satisfy the setup and hold times t_{16} and t_{17} for proper chip operation.

1.5 Pin Description (Continued)

Symbol	Type	Name and Function
BURST CONTROL		
BRDY#	I	The **burst ready** input performs the same function during a burst cycle that RDY# performs during a non-burst cycle. BRDY# indicates that the external system has presented valid data in response to a read for that the external system has accepted data in response to a write. BRDY# is ignored when the bus is idle and at the end of the first clock in a bus cycle. BRDY# is sampled in the second and subsequent clocks of a burst cycle. The data presented on the data bus will be strobed into the microprocessor when BRDY# is sampled active. If RDY# is returned simultaneously with BRDY#, BRDY# is ignored and the burst cycle is prematurely aborted. BRDY# is active LOW and is provided with a small pullup resistor. BRDY# must satisfy the setup and hold times t_{16} and t_{17}.
BLAST#	O	The **burst last** signal indicates that the next time BRDY# is returned the burst bus cycle is complete. BLAST# is active for both burst and non-burst bus cycles. BLAST# is active LOW and is not driven during bus hold.
INTERRUPTS		
RESET	I	The **reset** input forces the Low Power Intel486 microprocessor to begin execution at a known state. The microprocessor cannot begin execution of instructions until at least 1 ms after V_{CC} and CLK2 have reached their proper D.C. and A.C. specifications. The RESET pin should remain active during this time to insure proper microprocessor operation. However, for warm boot-ups RESET should remain active for at least 30 CLK2 periods. RESET is active HIGH. RESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
INTR	I	The **maskable interrupt** indicates that an external interrupt has been generated. If the internal interrupt flag is set in EFLAGS, active interrupt processing will be initiated. The Low Power Intel486 microprocessor will generate two locked interrupt acknowledge bus cycles in response to the INTR pin going active. INTR must remain active until the interrupt acknowledges have been performed to assure that the interrupt is recognized. INTR is active HIGH and is not provided with an internal pulldown resistor. INTR is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
NMI	I	The **non-maskable interrupt** request signal indicates that an external non-maskable interrupt has been generated. NMI is rising edge sensitive. NMI must be held LOW for at least eight CLK2 periods before this rising edge. NMI is not provided with an internal pulldown resistor. NMI is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
BUS ARBITRATION		
BREQ	O	The **internal cycle pending** signal indicates that the Low Power Intel486 microprocessor has internally generated a bus request. BREQ is generated whether or not the Low Power Intel486 microprocessor is driving the bus. BREQ is active high and is never floated.
HOLD	I	The **bus hold request** allows another bus master complete control of the Low Power Intel486 microprocessor bus. In response to HOLD going active the Low Power Intel486 microprocessor will float most of its output and input/output pins HLDA will be asserted after completing the current bus cycle, burst cycle or sequence of locked cycles. The Low Power Intel486 microprocessor will remain in this state until HOLD is deasserted. HOLD is active high and is not provided with an internal pulldown resistor. HOLD must satisfy setup and hold times t_{18} and t_{19} for proper operation.

1.5 Pin Description (Continued)

Symbol	Type	Name and Function
BUS ARBITRATION (Continued)		
HLDA	O	**Hold acknowledge** goes active in response to a hold request presented on the HOLD pin. HDLA indicates that the Low Power Intel486 microprocessor has given the bus to another local bus master. HLDA is driven active in the same clock that the Low Power Intel486 microprocessor floats its bus. HLDA is driven inactive when leaving bus hold. HLDA is active HIGH and remains driven during bus hold.
BOFF#	I	The **backoff** input forces the Low Power Intel486 microprocessor to float its bus in the next clock. The microprocessor will float all pins normally floated during hold but HLDA will not be asserted in response to BOFF#. BOFF# has higher priority than RDY# or BRDY#; if both are returned in the same clock, BOFF# takes effect. The microprocessor remains in bus hold until BOFF# is negated. If a bus cycle was in progress when BOFF# was asserted the cycle will be restarted. BOFF# is active LOW and must meet setup and hold times t_{18} and t_{19} for proper operation.
CACH INVALIDATION		
AHOLD	I	The **address** hold request allows another bus master access to the Low Power Intel486 microprocessor's address bus for a cache invalidation cycle. The Low Power Intel486 microprocessor will stop driving its address bus in the clock following AHOLD going active. Only the address bus will be floated during address hold, the remainder of the bus will remain active. AHOLD is active HIGH and is provided with a small internal pulldown resistor. For proper operation AHOLD must meet setup and hold times t_{18} and t_{19}.
EADS#	I	This signal indicates that a valid **external address** has been driven onto the Low Power Intel486 microprocessor address pins. This address will be used to perform an internal cache invalidation cycle. EADS# is active LOW and is provided with an internal pullup resistor. EADS# must satisfy setup and hold times t_{12} and t_{13} for proper operation.
CACHE CONTROL		
KEN#	I	The **cache enable** pin is used to determine whether the current cycle is cacheable. When the Low Power Intel486 microprocessor generates a cycle that can be cached and KEN# is active, the cycle will become a cache line fill cycle. Returning KEN# active one clock before ready during the last read in the cache line fill will cause the line to be placed in the on-chip cache. KEN# is active LOW and is provided with a small internal pull-up resistor. KEN# must satisfy setup and hold times t_{14} and t_{15} for proper operation.
FLUSH#	I	The **cache flush** input forces the Low Power Intel486 microprocessor to flush its entire internal cache. FLUSH# is active low and need only be asserted for one clock. FLUSH# is asynchronous but setup and hold times t_{20} and t_{21} must be met for recognition in any specific clock. FLUSH# being sampled low in the clock before the falling edge of RESET causes the Low Power Intel486 microprocessor to enter the tri-state test mode.
PAGE CACHEABILITY		
PWT PCD	O O	The **page write-through** and **page cache disable** pins reflect the state of the page attribute bits, PWT and PCD, in the page table entry, page directory entry or control register 3 (CR3), when paging is enabled. If paging is disabled, the CPU ignores the PCD and PWT bits and assumes they are zero for the purpose of caching and driving PCD and PWT pins. PWT and PCD have the same timing as the cycle definition pins (M/IO#, D/C#, and W/R#). PWT and PCD are active HIGH and are not driven during bus hold. PCD is masked by the cache disable bit (CD) in Control Register 0.

1.5 Pin Description (Continued)

Symbol	Type	Name and Function
NUMERIC ERROR REPORTING (Present on Intel486 DX CPU Only)		
FERR#	O	The **floating point error** pin is driven active when a floating point error occurs. FERR# is similar to the ERROR# pin on the i387 Math CoProcessor. FERR# is included for compatibility with systems using DOS type floating point error reporting. FERR# is active LOW, and is not floated during bus hold.
IGNNE#	I	When the **ignore numeric error** pin is asserted, the Low Power Intel486 microprocessor will ignore a numeric error and continue executing non-control floating point instructions. When IGNNE# is deasserted the Low Power Intel486 microprocessor will freeze on a non-control floating point instruction, if a previous floating point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set. IGNNE# is active LOW and is provided with a small internal pullup resistor. IGNNE# is asynchronous but setup and hold times t_{20} and t_{21} must be met to insure recognition on any specific clock.
BUS SIZE CONTROL		
BS16# BS8#	I I	The **bus size 16** and **bus size 8** pins (bus sizing pins) cause the Low Power Intel486 microprocessor to run multiple bus cycles to complete a request from devices that cannot provide or accept 32 bits of data in a single cycle. The bus sizing pins are sampled every clock. The state of these pins in the clock before ready is used by the Low Power Intel486 microprocessor to determine the bus size. These signals are active LOW and are provided with internal pullup resistors. These inputs must satisfy setup and hold times t_{14} and t_{15} for proper operation.
ADDRESS MASK		
A20M#	I	When the **address bit 20 mask** pin is asserted, the Low Power Intel486 microprocessor masks physical address bit 20 (A20) before performing a lookup to the internal cache or driving a memory cycle on the bus. A20M# emulates the address wraparound at one Mbyte which occurs on the 8086. A20M# is active LOW and should be asserted only when the processor is in real mode. This pin is asynchronous but should meet setup and hold times t_{20} and t_{21} for recognition in any specific clock. For proper operation, A20M# should be sampled high at the falling edge of RESET.
PERFORMANCE UPGRADE SUPPORT (Intel486 SX CPU PQFP Version Only)		
UP#	I	*Upgrade Present* forces the Intel486 SX CPU to tri-state all its outputs and enter the power down mode. UP# is active low and is sampled at all times, including after power-up and during reset.
TEST ACCESS PORT (Intel486 SX CPU PQFP Version Only)		
TCK	I	*Test Clock* is an input to the Intel486™ CPU and provides the clocking function required by the JTAG Boundary scan feature. TCK is used to clock state information and data into component on the rising edge of TCK on TMS and TDI, respectively. Data is clocked out of the part on the falling edge of TCK and TDO.
TDI	I	*Test Data Input* is the serial input used to shift JTAG instructions and data into component. TDI is sampled on the rising edge of TCK, during the SHIFT-IR and SHIFT-DR TAP controller states. During all other tap controller states, TDI is a "don't care".
TDO	O	*Test Data Output* is the serial output used to shift JTAG instructions and data out of the component. TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR TAP controller states. At all other times TDO is driven to the high impedance state.
TMS	I	*Test Mode Select* is decoded by the JTAG TAP (Tap Access Port) to select the operation of the test logic. TMS is sampled on the rising edge of TCK. To guarantee deterministic behavior of the TAP controller TMS is provided with an internal pull-up resistor.

OUTPUT PINS

Table 1-1. lists all the output pins, indicating their active level, and when they are floated.

Table 1-1. Output Pins

Name	Active Level	When Floated
BREQ	HIGH	
HLDA	HIGH	
BE0#–BE3#	LOW	Bus Hold
PWT, PCD	HIGH	Bus Hold
W/R#, D/C#, M/IO#	HIGH/LOW	Bus Hold
LOCK#	LOW	Bus Hold
PLOCK#	LOW	Bus Hold
ADS#	LOW	Bus Hold
BLAST#	LOW	Bus Hold
PCHK#	LOW	
FERR#*	LOW	
A2-A3	HIGH	Bus, Address Hold

*Present on Intel486 DX CPU Only

INPUT PINS

Table 1-2 lists all input pins, indicating their active level, and whether they are synchronous or asynchronous inputs.

Table 1-2. Input Pins

Name	Active Level	Synchronous/ Asynchronous
CLK2		
CLKSEL		
RESET	HIGH	Asynchronous
HOLD	HIGH	Synchronous
AHOLD	HIGH	Synchronous
EADS#	LOW	Synchronous
BOFF#	LOW	Synchronous
FLUSH#	LOW	Asynchronous
A20M#	LOW	Asynchronous
BS16#, BS8#	LOW	Synchronous
KEN#	LOW	Synchronous
RDY#	LOW	Synchronous
BRDY#	LOW	Synchronous
INTR	HIGH	Asynchronous
NMI	HIGH	Asynchronous
IGNNE#*(1)	LOW	Asynchronous
UP#(2)	LOW	Asynchronous

NOTES:
1. The IGNNE# pin is present on the Intel486 DX CPU and Intel487 SX MCP only.
2. The UP# pin is present on the Intel486 SX CPU PQFP package only.

INPUT/OUTPUT PINS

Table 1-3 lists all the input/output pins, indicating their active level and when they are floated.

Table 1-3. Input/Output Pins

Name	Active Level	When Floated
D0–D31	HIGH	Bus Hold
DP0–DP3	HIGH	Bus Hold
A4–A31	HIGH	Bus, Address Hold

Table 1-4. Test Pins

Name	Input or Output	Sampled/ Driven On
TCK	Input	N/A
TDI	Input	Rising Edge of TCK
TDO	Output	Falling Edge of TCK
TMS	Input	Rising Edge of TCK

Table 1-5. Component and Revision ID (PGA)

I486 SX Microprocessor/ I487 SX Math CoProcessor Stepping Name	Component ID	Revision ID
A0	04	20

NOTE:
Table 1-5 shows the Component ID number and Revision ID number for the A-0 stepping of the Intel486 SX Microprocesor and Intel487 SX Math CoProcessor. When an Intel487 SX Math CoProcessor is installed in the system, the Component ID and Revision ID is provided by the Intel487 SX Math CoProcessor and not the Intel486 SX Microprocessor. The Component ID and Revision ID read by the BIOS/software may change when a Performance Upgrade Component, such as the Intel487 SX Math CoProcessor, is installed in an Intel486 SX Microprocessor based system.

1.6 Signal Description

With the exception of CLK2 and CLKSEL, all signals follow the same definition as the Intel486 microprocessor. The A.C. timing parameters for all of these signals are given in Table 2-7.

CLOCK (CLK2)

CLK2 provides the fundamental timing for the Low Power Intel486 microprocessor. It is divided by two internally to generate the internal processor clock used for instruction execution. The internal clock is comprised of two phases, "phase one" and "phase two". Each CLK2 period is a phase of the internal clock. Figure 1-5 illustrates the relationship. If de-

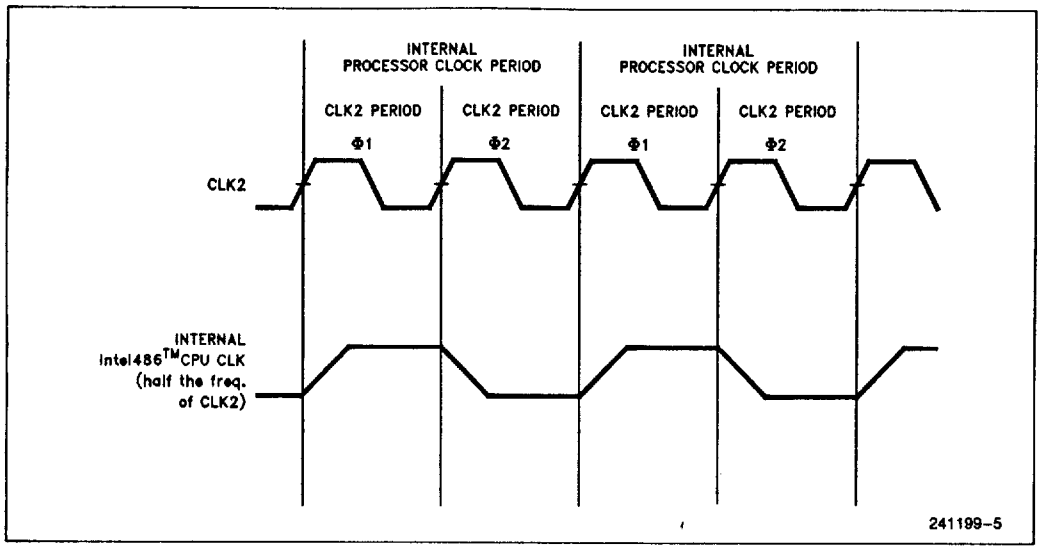


Figure 1-5. CLK2 Signal and Internal Processor Clock

sired, the phase of the internal processor clock can be synchronized to a known phase by ensuring the pulse on the CLKSEL pin meets the applicable timings during cold boot (power-up reset).

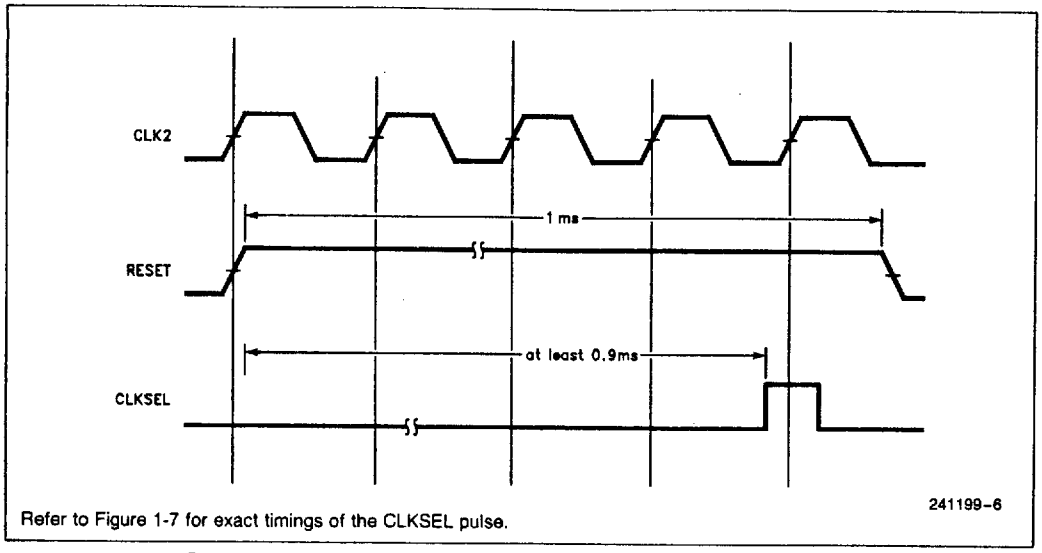
All set-up, hold, float-delay and valid delay timings are referenced to the phase one of the clock.

The internal processor clock (CLK) is similar to the clock signal of the standard Intel486 microprocessor. All I/O signals get sampled on the rising edge of this signal, i.e. the rising edge of phase one. Thus it is important to synchronize the external circuitry with the phase one of CLK2.

CLKSEL

Clock Select pin selects the 2X mode required for the Low Power Intel486 CPU. This pin should be driven low after power-up and during the entire operation of the CPU. However, a well defined pulse is required on CLKSEL pin during cold boot (power-up reset) to establish the phase relationship of the 2X clock. The reset pulse width during cold reset should be at least 1 ms. As shown in Figure 1-6, the pulse on CLKSEL should be asserted by the end of reset (approximately 0.9 ms after driving reset active) and at least 30 CLK2 periods before the falling edge of reset.

Figure 1-7 shows the detailed timing definition of this pulse. The pulse on CLKSEL pin is only required during power-up reset. During all other times including warm resets the CLKSEL pin should be driven low and must be free of spikes or glitches. After the power-up reset, the system must track the phase of CLK2 at all times including during warm resets so that the input/output signals can be sampled at the appropriate clock edge. The phase relationship is described in the next section.



Refer to Figure 1-7 for exact timings of the CLKSEL pulse.

Figure 1-6. CLKSEL Pulse with Reference to the Reset Pulse Width

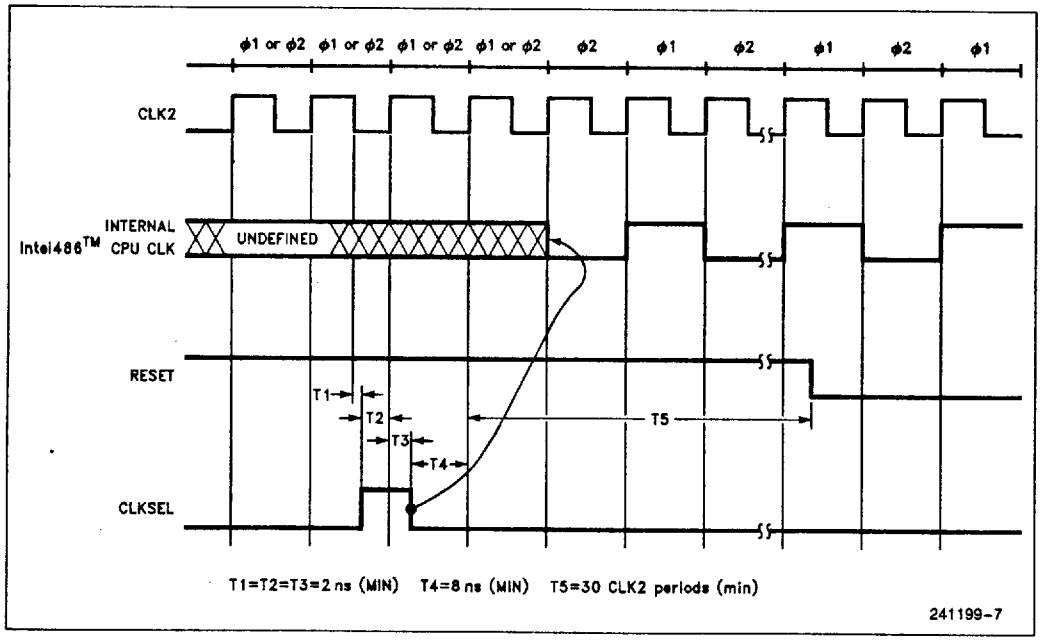


Figure 1-7. CLKSEL Timing Definition during Power-Up Reset

1.7 Architecture Overview

The Low Power Intel486 microprocessor is architecturally similar to the Intel486 CPU. Thus all bus cycles follow the same definition (for details see the Intel486 data sheet). The difference lies in the fact that the Low Power Intel486 CPU works with an external 2X clock input (CLK2). As shown in Figure 1-5, each of the internal processor clock (CLK) cycle is two CLK2 cycles wide. Thus a 25 MHz Low Power Intel486 microprocessor needs a 50 MHz clock input.

CLK2 provides the fundamental timing for the Low Power Intel486 CPU. It is divided by two internally to generate the internal processor clock (CLK) used for instruction execution. The internal clock is comprised of two phases, "phase one" and "phase two". Each CLK2 period is a phase of the internal clock. All Low Power Intel486 microprocessor inputs are sampled at the rising edge of phase 1. Each bus cycle is comprised of at least two bus states, T1 and T2. Each bus state in turn consists of two CLK2 cycles phase 1 and phase 2 of the bus state. The bus state diagram in Section 7.2.13 of the Intel486 CPU data sheet is valid for the Low Power Intel486 microprocessor.

NOTE:
The timing diagrams given in the Intel486 data sheet can be used for the Low Power Intel486 microprocessor. Read "CLK" signal as the internal clock of the CPU, with "CLK2" (the input clock of the Low Power Intel486 CPU) being twice the frequency of the internal processor clock as shown in Figure 1-5.

The following describes how the input signals are sampled and output signals are referenced with respect to the input clock (CLK2):

INPUT SIGNALS:

The Low Power Intel486 CPU samples all its **synchronous** input signals (i.e. RDY#, BRDY#, BS8#, BS16#, KEN#, EADS#, BOFF#, HOLD and AHOLD) at the rising edge of phase 1, as long as proper setup and hold times relative to that clock edge are met.

The Low Power Intel486 CPU samples all its **asynchronous** input signals (i.e. RESET, INTR, NMI, A20M# FLUSH#, IGNNE#) at every other rising edge of the system clock (Phase 1), as long as proper setup and hold times relative to that clock edge are met.

OUTPUT SIGNALS

The A.C. timing specifications for output signals (i.e. valid and float delay timings) are specified with respect to the rising edge of the Phase 1 of the system clock. This holds true for all output signals including ADS# and PCHK#.

1.8 Variable CPU Frequency

The Low Power Intel486 microprocessor allows the CPU frequency to change dynamically. As shown in Figures 1-8 and 1-9, the relationship between frequency and power consumption is approximately linear. Thus lowering the CPU frequency, reduces the power supply current (I_{CC}) consumed by the CPU.

The following must be satisified to change the CPU frequency:

1. Frequency can be changed at least 8 clocks after satisfying t4 (see Figure 1-7). The system can be started at a lower frequency and after satisfying the CLKSEL pulse specifications, it can be operated at the required speed.
2. The change in frequency should satisfy the minimum specification of "CLK2 high time" and "CLK2 low time". That is, at no time should the clock period go below the specified clock high and clock low times (see A.C. specifications for exact values).

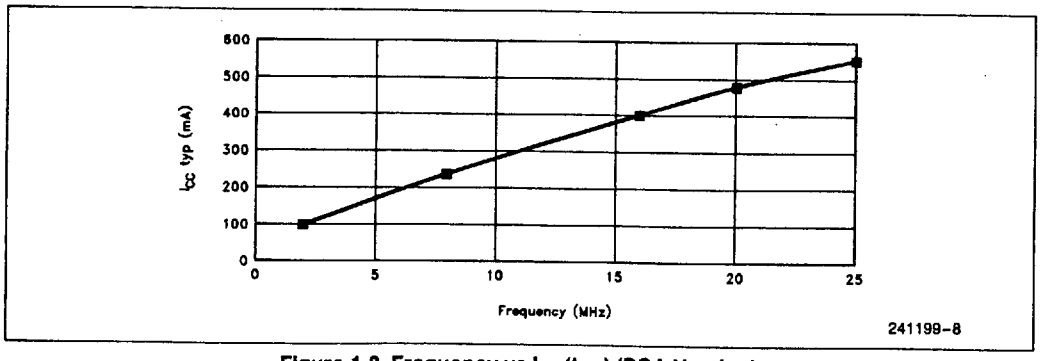


Figure 1-8. Frequency vs I_{CC}(typ) (PGA Version)

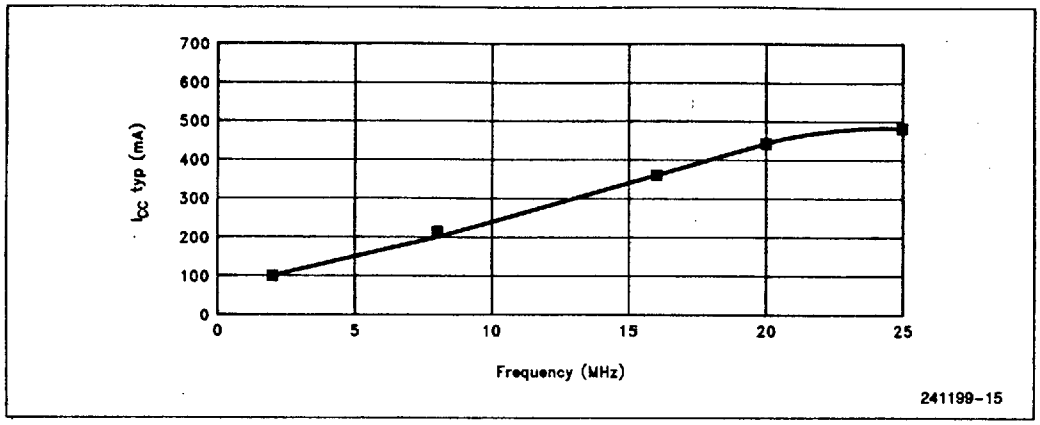


Figure 1-9. Frequency vs I_{CC}(typ) (PQFP Version)

2.0 D.C./A.C. SPECIFICATIONS

Table 2-1 provides the absolute maximum ratings. It is a stress rating only and functional operation at the maximums is not guaranteed. Functional operating conditions are given in Section 2.1 D.C. Specifications and 2.3 A.C. Specifications.

Table 2-1. Absolute Maximum Ratings

Case Temperature under Bias	−65°C to +110°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin with Respect to Ground	−0.5V to (V_{CC} +0.5V)
Supply Voltage with Respect to V_{SS}	−0.5V to +6.5V

2.1 D.C. Specifications

Table 2-2 provides the D.C. operating conditions for the Low Power Intel486 DX microprocessor.

Functional operating range: V_{CC} = 5V ±10%; T_{case} = 0°C to +85°C.

Table 2-2. Low Power Intel486 DX Microprocessor D.C. Parametric Values (PGA Version)

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	−0.3	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage		0.45	V	(Note 1)
V_{OH}	Output High Voltage	2.4		V	(Note 2)
I_{CC}	Power Supply Current CLK2 = 50 MHz		700	mA	(Note 3)
I_{LI}	Input Leakage Current		±15	μA	(Note 4)
I_{IH}	Input Leakage Current		200	μA	(Note 5)
I_{IL}	Input Leakage Current		−400	μA	(Note 6)
I_{LO}	Output Leakage Current		±15	μA	
C_{IN}	Input Capacitance		20	pF	F_c = 1 MHz(7)
C_O	I/O or Output Capacitance		20	pF	F_c = 1 MHz(7)
C_{CLK}	CLK Capacitance		20	pF	F_c = 1 MHz(7)

NOTES:
1. This parameter is measured at:
   Address, Data BEn 4.0 mA
   Definition, Control 5.0 mA
2. This parameter is measured at:
   Address, Data BEn −1.0 mA
   Definition, Control −0.9 mA
3. Typical supply current
   I_{CC} = 550 mA @CLK2 = 50 MHz
4. This parameter is for inputs without pullups or pulldowns and $0 \le V_{IN} \le V_{CC}$.
5. This parameter is for inputs with pulldowns and V_{IH} = 2.4V.
6. This parameter is for inputs with pullups and V_{IL} = 0.45V.
7. Not 100% tested.

Table 2-3 provides the D.C. operating conditions for the Low Power Intel486 SX microprocessor (PGA Version) and the Intel487 SX Math CoProcessor installed in a low power system.

Functional Operating Range: V_{CC} = 5V ±10%; T_{case} = 0°C to +85°C.

Table 2-3. Low Power Intel486 SX Microprocessor D.C. Parametric Values (PGA Version)

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	−0.3	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage		0.45	V	(Note 1)
V_{OH}	Output High Voltage	2.4		V	(Note 2)
I_{CC}	Power Supply Current CLK2 = 32 MHz = 40 MHz = 50 MHz		 525 600 700	mA	(Note 3)
I_{CCF}	Power Supply Current with Intel486 SX CPU Tri-stated (floating) CLK2 = 32 MHz = 40 MHz = 50 MHz		 400 500 600	mA	
I_{LI}	Input Leakage Current		±15	µA	(Note 4)
I_{IH}	Input Leakage Current		200	µA	(Note 5)
I_{IL}	Input Leakage Current		−400	µA	(Note 6)
I_{LO}	Output Leakage Current		±15	µA	
C_{IN}	Input Capacitance		20	pF	F_c = 1 MHz(7)
C_O	I/O or Output Capacitance		20	pF	F_c = 1 MHz(7)
C_{CLK}	CLK Capacitance		20	pF	F_c = 1 MHz(7)

NOTES:
1. This parameter is measured at:
   Address, Data BEn 4.0 mA
   Definition, Control 5.0 mA
2. This parameter is measured at:
   Address, Data BEn −1.0 mA
   Definition, Control −0.9 mA
3. Typical supply current
   I_{CC} = 400 @CLK2 = 32 MHz (Normal Operation)
   = 475 mA @CLK2 = 40 MHz
   = 500 mA @CLK2 = 50 MHz
   I_{CCF} = 325 mA @CLK2 = 32 MHz Intel486 CPU Tri-stated (Floating)
   = 400 mA @CLK2 = 40 MHz
   = 470 mA @CLK2 = 50 MHz
4. This parameter is for inputs without pullups or pulldowns and $0 \le V_{IN} \le V_{CC}$.
5. This parameter is for inputs with pulldowns and V_{IH} = 2.4V.
6. This parameter is for inputs with pullups and V_{IL} = 0.45V.
7. Not 100% tested.

Table 2-4 provides the D.C. Operating Conditions for the Low Power Intel486 SX microprocessor (PQFP version) and the Intel487 SX Math CoProcessor installed in a low power system.

Functional Operating Range:

V_{CC} = 5V − 10%, +5%;
T_{CASE} = 0°C to +85°C

Table 2-4. Low Power Intel486™ SX Microprocessor D.C. Parametric Values (PQFP version)

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	−0.3	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage		0.45	V	(Note 1)
V_{OH}	Output High Voltage	2.4		V	(Note 2)
I_{CC}	Power Supply Current CLK2 = 32 MHz CLK2 = 40 MHz CLK2 = 50 MHz		 450 500 560	 mA	(Note 3)
I_{CCF}	Power Supply Current with Intel486 SX CPU in Power Down Mode		50	mA	(Note 7)
I_{LI}	Input Leakage Current		±15	μA	(Note 4)
I_{IH}	Input Leakage Current		200	μA	(Note 5)
I_{IL}	Input Leakage Current		−400	μA	(Note 6)
I_{LO}	Output Leakage Current		±15	μA	
C_{IN}	Input Capacitance		10	pF	F_C = 1 MHz (Note 7)
C_O	I/O or Output Capacitance		10	pF	F_C = 1 MHz (Note 7)
C_{CLK}	CLK Capacitance		6	pF	F_C = 1 MHz (Note 7)

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NOTES:
1. This parameter is measured at:
   Address, Data, BEn 4.0 mA
   Definition, Control 5.0 mA
2. This parameter is measured at:
   Address, Data BEn −1.0 mA
   Definition, Control −0.9 mA
3. Typical supply current:
   I_{CC} 380 mA @ CLK2 = 32 MHz (Normal Operation)
   440 mA @ CLK2 = 40 MHz
   480 mA @ CLK2 = 50 MHz
4. This parameter is for inputs without pullups or pulldowns and $0 \le V_{IN} \le V_{CC}$.
5. This parameter is for inputs with pulldowns and V_{IH} = 2.4V.
6. This parameter is for inputs with pullups and V_{IL} = 0.45V.
7. Not 100% tested.

2.2 Power Supply Current vs Frequency

Following is the power consumption of the Low Power Intel486 microprocessor or Intel487 Math CoProcessor installed in a low power system for different frequencies.

Table 2-5. Power Supply Current (I_{CC}) Values over Frequencies of Operation (PGA Version)

CLK2 Frequency (MHz)	Operating Frequency (MHz)	$I_{CC(max)}$ (mA)	$I_{CC(typ)}$ (mA)
4	2	150	100
16	8	325	235
32	16	525	400
40	20	600	475
50	25	700	550

Table 2-6. Power Supply Current (I_{CC}) Values over Frequencies of Operation (PQFP Version)

CLK2 Frequency (MHz)	Operating Frequency (MHz)	I_{CC} (max) (mA)	I_{CC} (typ) (mA)
4	2	150	100
16	8	250	210
32	16	450	380
40	20	500	440
50	25	560	480

2.3 A.C. Specifications

The following tables provide the A.C. specifications for the Low Power Intel486 microprocessors. They consist of output delays, input setup requirements and input hold requirements. All A.C. specifications are relative to the rising edge of the phase 1 of the input system clock (CLK2), unless otherwise specified.

Table 2-7. Low Power Intel486 DX—25 MHz Microprocessor A.C. Characteristics

V_{CC} = 5V ±10%; T_{case} = 0°C to +85°C; C_L = 50 pF(2) unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	2	25	MHz		Half of CLK2 Frequency
t_1	CLK2 Period	20	250	ns	2.1	
t_2	CLK2 High Time	7		ns	2.1	At 2V
t_3	CLK2 Low Time	7		ns	2.1	At 0.8V
t_4	CLK2 Fall Time		2	ns	2.1	2V to 0.8V
t_5	CLK2 Rise Time		2	ns	2.1	0.8V to 2V
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BREQ, HLDA Valid Delay	3	22	ns	2.2	
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK# Float Delay		30	ns	2.2	After Clock Edge(1)
t_8	PCHK# Valid Delay	3	27	ns	2.2	
t_{8a}	BLAST#, PLOCK# Valid Delay	3	27	ns	2.3	

Table 2-7. Low Power Intel486 DX—25 MHz Microprocessor A.C. Characteristics (Continued)
V_{CC} = 5V ±10%; T_{case} = 0°C to +85°C; C_L = 50 pF(2) unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_9	BLAST#, PLOCK# Float Delay		30	ns	2.2	After Clock Edge(1)
t_{10}	D0–D31, DP0–3 Write Data Valid Delay	3	22	ns	2.2	
t_{11}	D0–D31, DP0–3 Write Data Float Delay		30	ns	2.2	After Clock Edge(1)
t_{12}	EADS# Setup Time	9		ns	2.3	
t_{13}	EADS# Hold Time	4		ns	2.3	
t_{14}	KEN#, BS16#, BS8# Setup Time	9		ns	2.3	
t_{15}	KEN#, BS16#, BS8# Hold Time	4		ns	2.3	
t_{16}	RDY#, BRDY# Setup Time	9		ns	2.3	
t_{17}	RDY#, BRDY# Hold Time	4		ns	2.3	
t_{18}	HOLD, AHOLD, BOFF# Setup Time	11		ns	2.3	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	4		ns	2.3	
t_{20}	RESET, FLUSH#, A20M#, NMI, INTR, IGNNE# Setup Time	11		ns	2.3	
t_{21}	RESET, FLUSH#, A20M#, NMI, INTR, IGNNE# Hold Time	4		ns	2.3	
t_{22}	D0–D31, DP0–3, A4–A31 Read Setup Time	6		ns	2.3	
t_{23}	D0–D31, DP0–3, A4–A31 Read Hold Time	4		ns	2.3	
	CLKSEL	See Figures 1-6 and 1-7 for details on this signal. Figure 1-7 shows minimum timings required for the proper operation of the CPU. The pulse on CLKSEL can be of any length as long as the minimums are satisfied and the transitions from low to high occurs at the clock edge shown.				

NOTES:
1. Not 100% tested, guaranteed by design characterization.
2. All timing specifications assume C_L = 50 pF.

Table 2-8. Low Power Intel486™ SX—16 MHz Microprocessor/Intel487™ SX Math CoProcessor A.C. Characteristics

V_{CC} = 5V ±10%; T_{case} = 0°C to +85°C; C_L = 50 pF(2) unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	2	16	MHz		Half of CLK2 Frequency
t_1	CLK2 Period	31	250	ns	2.1	
t_2	CLK2 High Time	10		ns	2.1	At 2V
t_3	CLK2 Low Time	10		ns	2.1	At 0.8V
t_4	CLK2 Fall Time		4	ns	2.1	2V to 0.8V
t_5	CLK2 Rise Time		4	ns	2.1	0.8V to 2V
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, **FERR#***, BREQ, HLDA Valid Delay	3	26	ns	2.2	
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK# Float Delay		42	ns	2.2	After Clock Edge(1)
t_8	PCHK# Valid Delay	3	35	ns	2.2	
t_{8a}	BLAST#, PLOCK# Valid Delay	3	35	ns	2.2	
t_9	BLAST#, PLOCK# Float Delay		42	ns	2.2	After Clock Edge(1)
t_{10}	D0–D31, DP0–3 Write Data Valid Delay	3	30	ns	2.2	
t_{11}	D0–D31, DP0–3 Write Data Float Delay		42	ns	2.2	After Clock Edge(1)
t_{12}	EADS# Setup Time	12		ns	2.3	
t_{13}	EADS# Hold Time	4		ns	2.3	
t_{14}	KEN#, BS16#, BS8# Setup Time	12		ns	2.3	
t_{15}	KEN#, BS16#, BS8# Hold Time	4		ns	2.3	
t_{16}	RDY#, BRDY# Setup Time	12		ns	2.3	
t_{17}	RDY#, BRDY# Hold Time	4		ns	2.3	
t_{18}	HOLD, AHOLD, BOFF# Setup Time	12		ns	2.3	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	4		ns	2.3	
t_{20}	RESET, FLUSH#, A20M#, NMI, INTR, **IGNNE#*** Setup Time	14		ns	2.3	
t_{21}	RESET, FLUSH#, A20M#, NMI, INTR, **IGNNE#*** Hold Time	4		ns	2.3	
t_{22}	D0–D31, DP0–3, A4–A31 Read Setup Time	10		ns	2.3	
t_{23}	D0–D31, DP0–3, A4–A31 Read Hold Time	4		ns	2.3	
	CLKSEL	See Figures 1-6 and 1-7 for details on this signal. Figure 1-7 shows minimum timings required for the proper operation of the CPU. The pulse on CLKSEL can be of any length as long as the minimums are satisfied and the transitions from low to high occurs at the clock edge shown.				

*Present only in the Intel487 SX Math CoProcessor

Table 2-9. Low Power Intel486™ SX—20 MHz Microprocessor/Intel487™ SX Math CoProcessor A.C. Characteristics

V_{CC} = 5V ±10%; T_{case} = 0°C to +85°C; C_L = 50 pF(2) unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	2	20	MHz		Half of CLK2 Frequency
t_1	CLK2 Period	25	250	ns	2.1	
t_2	CLK2 High Time	8.5		ns	2.1	At 2V
t_3	CLK2 Low Time	8.5		ns	2.1	At 0.8V
t_4	CLK2 Fall Time		3	ns	2.1	2V to 0.8V
t_5	CLK2 Rise Time		3	ns	2.1	0.8V to 2V
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, **FERR#***, BREQ, HLDA Valid Delay	3	23	ns	2.2	
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK# Float Delay		37	ns	2.2	After Clock Edge(1)
t_8	PCHK# Valid Delay	3	28	ns	2.2	
t_{8a}	BLAST#, PLOCK# Valid Delay	3	28	ns	2.2	
t_9	BLAST#, PLOCK# Float Delay		37	ns	2.2	After Clock Edge(1)
t_{10}	D0–D31, DP0–3 Write Data Valid Delay	3	26	ns	2.2	
t_{11}	D0–D31, DP0–3 Write Data Float Delay		37	ns	2.2	After Clock Edge(1)
t_{12}	EADS# Setup Time	10		ns	2.3	
t_{13}	EADS# Hold Time	4		ns	2.3	
t_{14}	KEN#, BS16#, BS8# Setup Time	10		ns	2.3	
t_{15}	KEN#, BS16#, BS8# Hold Time	4		ns	2.3	
t_{16}	RDY#, BRDY# Setup Time	10		ns	2.3	
t_{17}	RDY#, BRDY# Hold Time	4		ns	2.3	
t_{18}	HOLD, AHOLD, BOFF# Setup Time	12		ns	2.3	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	4		ns	2.3	
t_{20}	RESET, FLUSH#, A20M#, NMI, INTR, **IGNNE#*** Setup Time	12		ns	2.3	
t_{21}	RESET, FLUSH#, A20M#, NMI, INTR, **IGNNE#*** Hold Time	4		ns	2.3	
t_{22}	D0–D31, DP0–3, A4–A31 Read Setup Time	6		ns	2.3	
t_{23}	D0–D31, DP0–3, A4–A31 Read Hold Time	4		ns	2.3	

*Present only in the Intel487 SX Math CoProcessor

NOTES:
1. Not 100% tested, guaranteed by design characterization.
2. All timing specifications assume C_L = 50 pF.

Table 2-10. Low Power Intel486—25 MHz Microprocessor/Intel487™ SX Math CoProcessor A.C. Characteristics

V_{CC} = 5V ±10%; T_{case} = 0°C to +85°C; C_L = 50 pF(2) unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	2	25	MHz		Half of CLK2 Frequency
t_1	CLK2 Period	20	250	ns	2.1	
t_2	CLK2 High Time	7		ns	2.1	At 2V
t_3	CLK2 Low Time	7		ns	2.1	At 0.8V
t_4	CLK2 Fall Time		2	ns	2.1	2V to 0.8V
t_5	CLK2 Rise Time		2	ns	2.1	0.8V to 2V
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, **FERR#***, BREQ, HLDA Valid Delay	3	19	ns	2.2	
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK# Float Delay		28	ns	2.2	After Clock Edge(1)
t_8	PCHK# Valid Delay	3	24	ns	2.2	
t_{8a}	BLAST#, PLOCK# Valid Delay	3	24	ns	2.2	
t_9	BLAST#, PLOCK# Float Delay		28	ns	2.2	After Clock Edge(1)
t_{10}	D0–D31, DP0–3 Write Data Valid Delay	3	20	ns	2.2	
t_{11}	D0–D31, DP0–3 Write Data Float Delay		28	ns	2.2	After Clock Edge(1)
t_{12}	EADS# Setup Time	9		ns	2.3	
t_{13}	EADS# Hold Time	4		ns	2.3	
t_{14}	KEN#, BS16#, BS8# Setup Time	9		ns	2.3	
t_{15}	KEN#, BS16#, BS8# Hold Time	4		ns	2.3	
t_{16}	RDY#, BRDY# Setup Time	9		ns	2.3	
t_{17}	RDY#, BRDY# Hold Time	4		ns	2.3	
t_{18}	HOLD, AHOLD, BOFF# Setup Time	11		ns	2.3	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	4		ns	2.3	
t_{20}	RESET, FLUSH#, A20M#, NMI, INTR, **IGNNE#*** Setup Time	11		ns	2.3	
t_{21}	RESET, FLUSH#, A20M#, NMI, INTR, **IGNNE#*** Hold Time	4		ns	2.3	
t_{22}	D0–D31, DP0–3, A4–A31 Read Setup Time	6		ns	2.3	

*Present only in the Intel487 SX Math CoProcessor

NOTES:
1. Not 100% tested, guaranteed by design characterization.
2. All timing specifications assume C_L = 50 pF.

Table 2-10. Low Power Intel486—25 MHz Microprocessor/Intel487™ SX Math CoProcessor A.C. Characteristics

V_{CC} = 5V ±10%; T_{case} = 0°C to +85°C; C_L = 50 pF(2) unless otherwise specified (Continued)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{23}	D0–D31, DP0–3, A4–A31 Read Hold Time	4		ns	2.3	
	CLKSEL	See Figures 1-6 and 1-7 for details on this signal. Figure 1-7 shows minimum timings required for the proper operation of the CPU. The pulse on CLKSEL can be of any length as long as the minimums are satisfied and the transitions from low to high occurs at the clock edge shown.				

*Present only in the Intel487 SX Math CoProcessor

NOTES:
1. Not 100% tested, guaranteed by design characterization.
2. All timing specifications assume C_L = 50 pF.

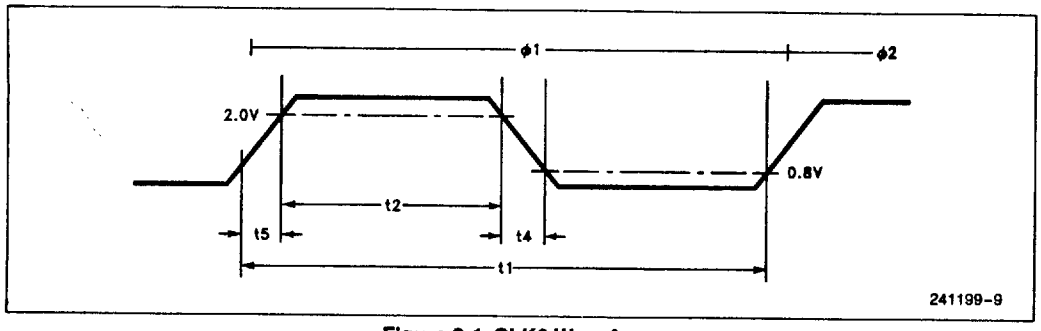

Figure 2-1. CLK2 Waveform

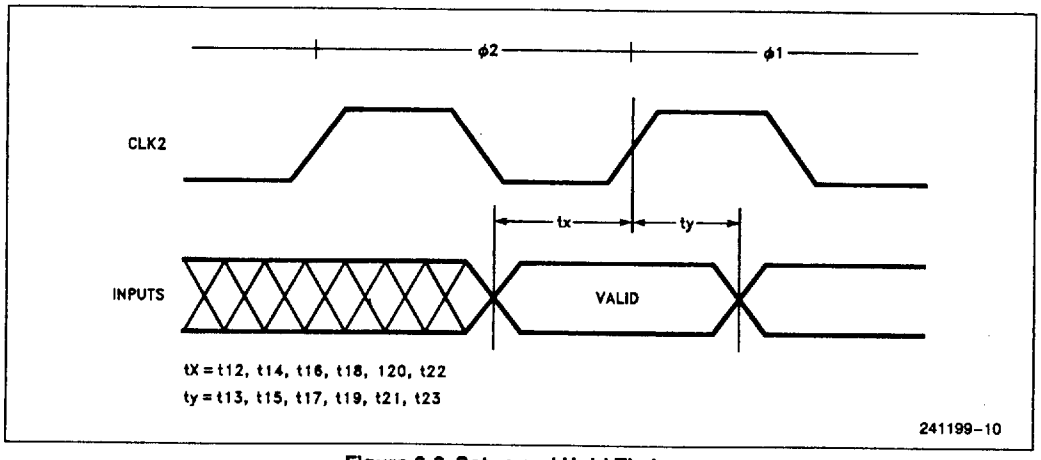

Figure 2-2. Setup and Hold Timings

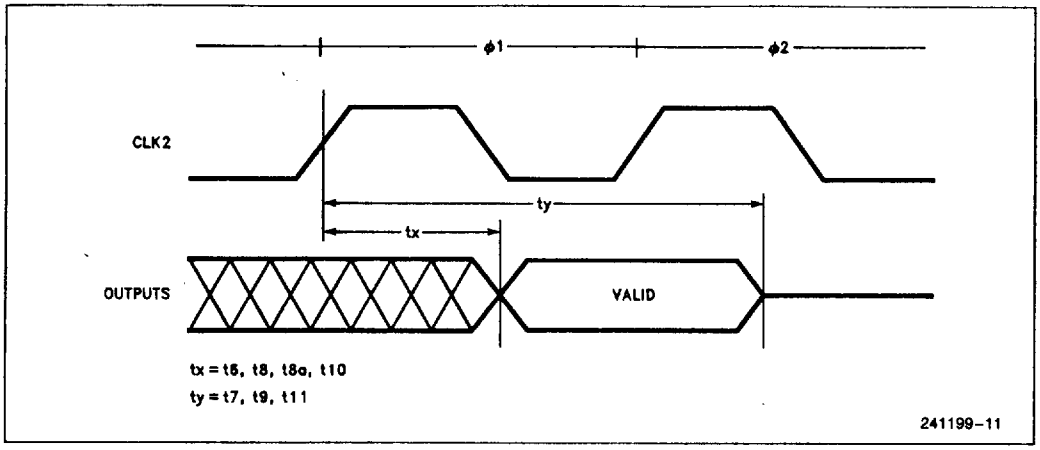

Figure 2-3. Valid and Float Delay Timings

3.0 MATH UPGRADE FOR LOW POWER Intel486™ SX MICROPROCESSOR

The Intel487 SX Math CoProcessor (MCP) is the math upgrade for the Low Power Intel486 SX microprocessor. The Intel487 SX MCP is designed and tested to operate with an external 1X clock input (standard mode) when it is installed in an Intel486 SX CPU system or with an external 2X clock input (low power mode) when it is installed in a Low Power Intel486 SX CPU based system. The Intel487 SX MCP is a super-set of the Intel486 SX CPU, containing a floating point unit, in addition to all other on-chip units present in the Intel486 SX microprocessor.

The Floating Point Unit (FPU) performs floating point operations on the 32-, 64-, and 80-bit arithmetic formats specified in IEEE Standard 754. Like the integer processing unit, the floating point unit architecture is binary-compatible with the 8087 and 80287 Math CoProcessors. The architecture is 100% compatible with the Intel287 and Intel387 Math CoProcessors.

The on-chip floating point unit of the Intel487 SX Math CoProcessor is similar to the FPU of the Intel486 DX CPU containing eight data registers, a tag word, a control register, a status register, an instruction pointer and a data pointer. (For details on FP registers and instructions, see the Intel486 SX CPU/Intel487 SX MCP data sheet Section 2.1.3).

Note that the Intel487 SX Math Coprocessor is the only upgrade available for the Low Power Intel486 SX microprocessor based designs. It is fully compatible with the Low Power mode of the Intel486 SX CPU. However, the Intel OverDrive Processor does not work in systems based on the Low Power Intel486 CPU. All address, data and control signals, including the external CPU clock input (CLK2) and the CLKSEL signal of the Low Power Intel486 SX CPU, must be tied to the corresponding signals of the Intel487 SX MCP (i.e. the Intel486 SX CPU's CLK2 signal must be connected to the Intel487 SX MCP's CLK2 signal, and the Intel486 SX CPU's CLKSEL signal must be connected to the CLKSEL signal on the Intel487 SX MCP). Additionally, the performance upgrade circuit given in the Intel486 SX CPU/Intel487 SX MCP data sheet should be followed to provide the math upgrade capability in Low Power Intel486 SX CPU systems.

The D.C./A.C. specifications given in Section 2.0 apply to the Low Power Intel486 SX CPU and the Intel487 SX MCP when it is installed in a Low Power Intel486 SX CPU system.

3.1 Pinout

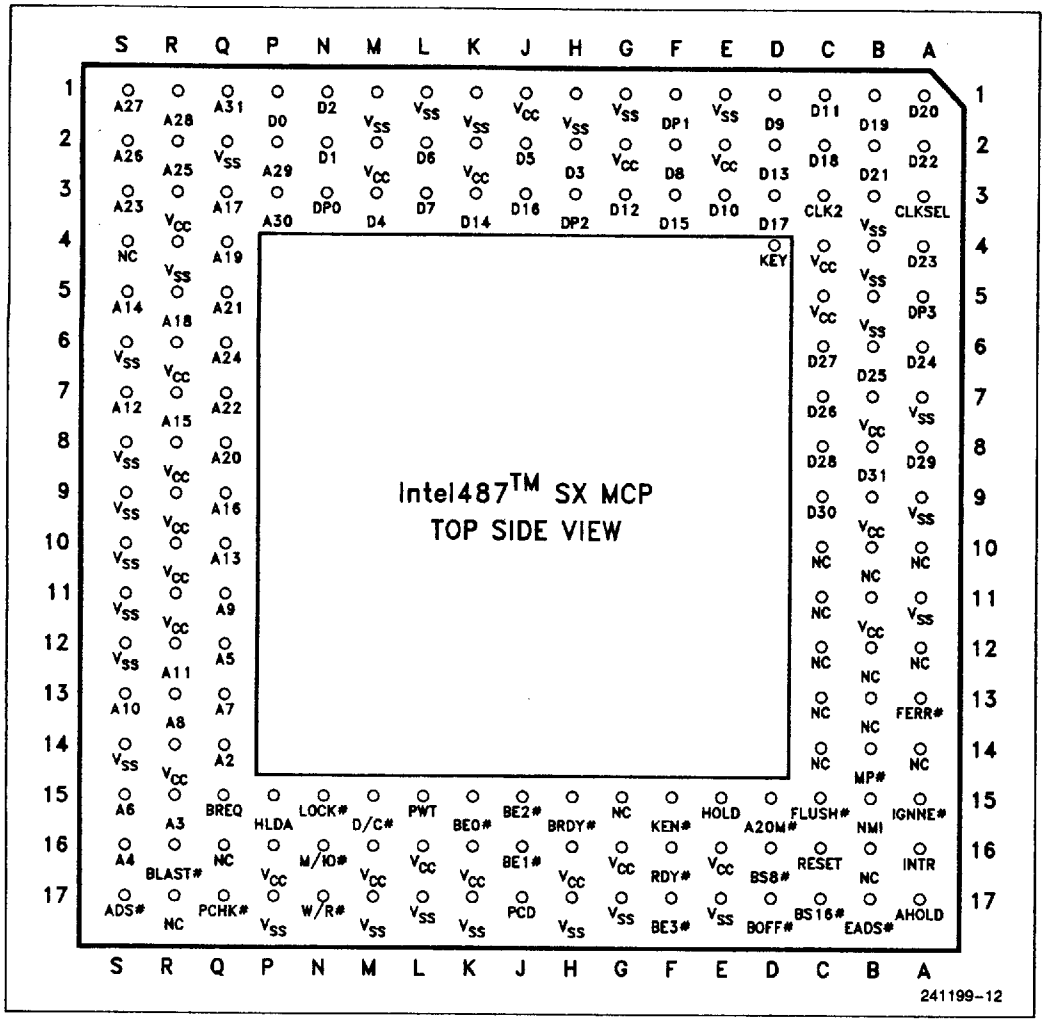

Figure 3-1. Intel487™ SX MCP Pinout for Low Power Designs (Top Side View)

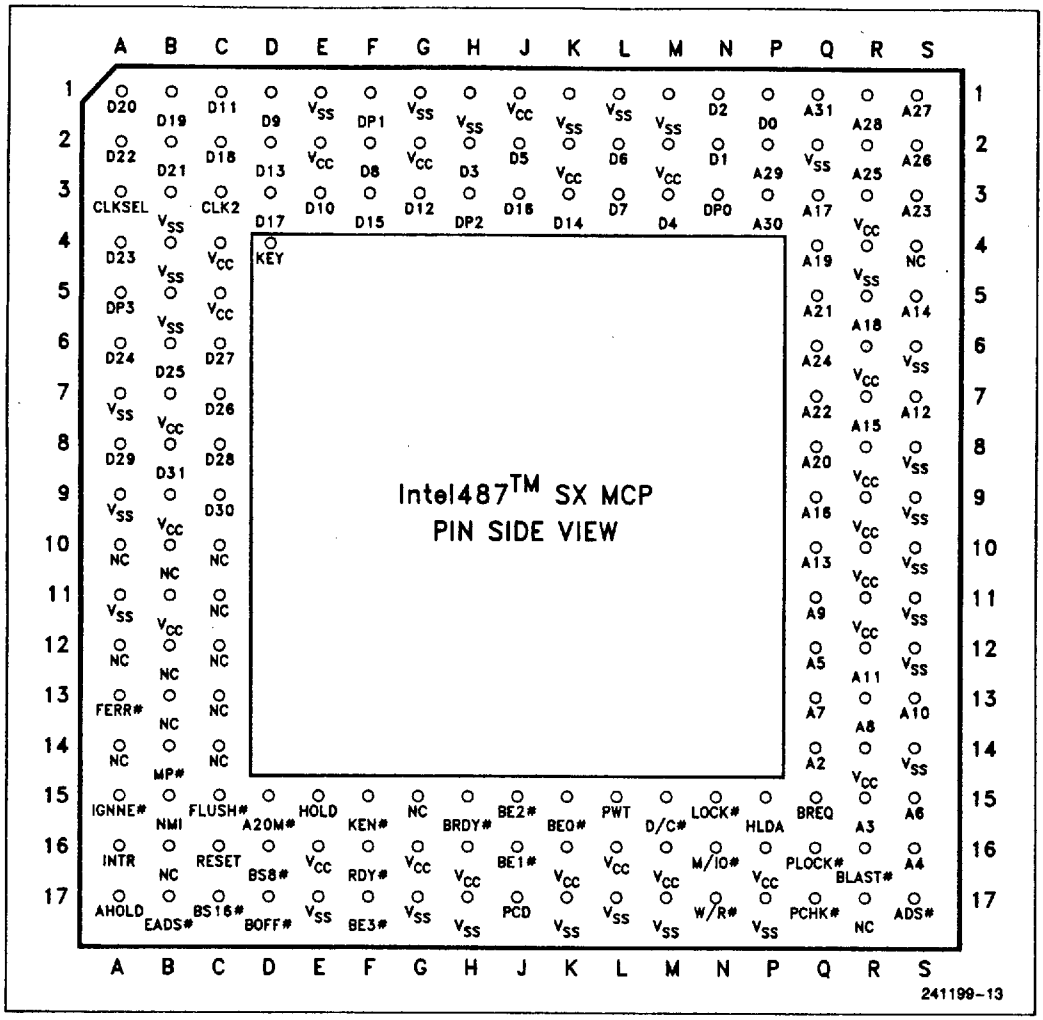

Figure 3-2. Intel487™ SX MCP Pinout for Low Power Designs (Pin Side View)

3.2. Pin Reference of Intel487™ SX Math CoProcessor

Table 3-1. Pin Cross Reference by Pin Name

Address		Data		Control		N/C	V_{CC}	V_{SS}
A_2	Q14	D_0	P1	A20M#	D15	A10	B7	A7
A_3	R15	D_1	N2	ADS#	S17	A12	B9	A9
A_4	S16	D_2	N1	AHOLD	A17	A14	B11	A11
A_5	Q12	D_3	H2	BE0#	K15	B10	C4	B3
A_6	S15	D_4	M3	BE1#	J16	B12	C5	B4
A_7	Q13	D_5	J2	BE2#	J15	B13	E2	B5
A_8	R13	D_6	L2	BE3#	F17	B16	E16	E1
A_9	Q11	D_7	L3	BLAST#	R16	C10	G2	E17
A_{10}	S13	D_8	F2	BOFF#	D17	C11	G16	G1
A_{11}	R12	D_9	D1	BRDY#	H15	C12	H16	G17
A_{12}	S7	D_{10}	E3	BREQ	Q15	C13	J1	H1
A_{13}	Q10	D_{11}	C1	BS8#	D16	C14	K2	H17
A_{14}	S5	D_{12}	G3	BS16#	C17	G15	K16	K1
A_{15}	R7	D_{13}	D2	CLK2	C3	R17	L16	K17
A_{16}	Q9	D_{14}	K3	CLKSEL	A3	S4	M2	L1
A_{17}	Q3	D_{15}	F3	D/C#	M15		M16	L17
A_{18}	R5	D_{16}	J3	DP0	N3		P16	M1
A_{19}	Q4	D_{17}	D3	DP1	F1		R3	M17
A_{20}	Q8	D_{18}	C2	DP2	H3		R6	P17
A_{21}	Q5	D_{19}	B1	DP3	A5		R8	Q2
A_{22}	Q7	D_{20}	A1	EADS#	B17		R9	R4
A_{23}	S3	D_{21}	B2	FERR#	A13		R10	S6
A_{24}	Q6	D_{22}	A2	FLUSH#	C15		R11	S8
A_{25}	R2	D_{23}	A4	HLDA	P15		R14	S9
A_{26}	S2	D_{24}	A6	HOLD	E15			S10
A_{27}	S1	D_{25}	B6	IGNNE#	A15			S11
A_{28}	R1	D_{26}	C7	INTR	A16			S12
A_{29}	P2	D_{27}	C6	KEN#	F15			S14
A_{30}	P3	D_{28}	C8	LOCK#	N15			
A_{31}	Q1	D_{29}	A8	M/IO#	N16			
		D_{30}	C9	MP#	B14			
		D_{31}	B8	NMI	B15			
				PCD	J17			
				PCHK#	Q17			
				PWT	L15			
				PLOCK#	Q16			
				RDY#	F16			
				RESET	C16			
				W/R#	N17			

3.3. Intel487™ SX Math CoProcessor Pin Description

The Intel487 SX Math CoProcessor consists of all the Intel486 SX microprocessor signals with the following additional pins.

NUMERIC ERROR REPORTING		
FERR#	O	The **Floating point error** pin is driven active when a floating point error occurs. FERR# is similar to the ERROR# pin on the i387 Math CoProcessor. FERR# is included for compatibility with systems using DOS type floating point error reporting. FERR# is active LOW, and is not floated CONT1g bus hold.
IGNNE#	I	When the **ignore numeric error** pin is asserted, the Low Power Intel487 SX Math CoProcessor will ignore a numeric error and continue executing non-control floating point instructions. When IGNNE# is deasserted the Low Power Intel487 SX Math CoProcessor will freeze on a non-control floating point instruction, if a previous floating point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set. IGNNE# is active LOW and is provided with a small internal pullup resistor. IGNNE# is asynchronous but setup and hold times t_{20} and t_{21} must be met to insure recognition on any specific clock.
Intel487™ SX MATH COPROCESSOR INTERFACE		
MP#	O	The **math present** pin is used to signal the Intel486 SX microprocessor to float its outputs and get-off the bus. This pin can be used to check the presence of the Math CoProcessor in the two socket math upgrade circuit. It is active low and is never floated. MP# is driven low at power-up and remains active for the entire duration of the Intel487™ SX Math CoProcessor operation.
KEY PIN		
KEY		The **KEY** pin is an electrically non-functional pin which is used to insure the correct Intel487 SX Math CoProcessor orientation in a 169-pin socket. KEY pin is located at "D4" and is the 169th pin of the Intel487 SX MCP.

4.0 REVISION HISTORY

Revision-002 of the Low Power Intel486 SX CPU/Intel487 SX MCP data book contains many updates and improvements to the original version. A revision summary of major changes is listed below:

The sections significantly revised since version -001 are:

Cover Page	Added Low Power Intel486 SX CPU PQFP package information.
Section 1.1	Added Figure 1-5. Low Power Intel486 SX CPU PQFP Pinout.
Section 1.4	Added Low Power Intel486 SX CPU PQFP package to Pin Cross Reference Table.
Section 1.5	Added Performance Upgrade Support section of Low Power Intel486 SX CPU PQFP package.
	Added Table 1-5. Test Pins.
	Added Table 1-6 Component ID and Revision ID.
	Added Test Access Port section of Low Power Intel486 SX CPU PQFP package.
Table 1-2	Noted IGNNE# pin is present on the Intel486 DX CPU and Intel487 SX MCP only.
	Added UP# pin and descriptions.
Section 1.7	Added Figure 1-9. Frequency vs I_{CC} (typ) (PQFP Version).
Section 2.1	Added Table 2-4. Intel486 SX Microprocessor D.C. Parametric Values (for PQFP package).
Section 2.2	Added Table 2-6 Power Supply Current (I_{CC}) Values over Frequencies of Operation (PQFP Version).

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